CLAIMS

What is claimed is:

1. A single flux quantum (SFQ) superconductive integrated circuit comprising:

a clock storage circuit for receiving and storing a load clock signal pulse; and

a data storage circuit coupled to said clock storage circuit for receiving and storing a data signal pulse in a sequential order, said data signal pulse being received relative to said load clock signal pulse, wherein said data-storage circuit outputs said data signal pulse independent of said load clock signal pulse.

2. The integrated circuit of claim 1 wherein said clock storage circuit receives a read clock signal pulse that is independent of said load clock signal pulse.

3. The integrated circuit of claim 1 wherein said clock storage circuit further includes:

a current source;

a plurality of first junctions coupled to said current source for receiving and storing said load clock signal pulse, wherein one of said plurality of first junctions defines an input port; and

an end junction coupled to one of said plurality of first junctions for receiving and storing said load clock signal pulse.

4. The integrated circuit of claim 3 wherein said load clock signal pulse propagates through said plurality of first junctions that are empty towards said end junction and occupies a last empty junction.

5. The integrated circuit of claim 3 wherein said read and load clock signal pulses are eliminated when said signal pulses are combined and said end junction is emptied.

6. The integrated circuit of claim 5 wherein each of said load clock signal pulses stored in said first junctions move down through said plurality of first junctions and said end junction that are empty towards said end junction in sequential order of said load clock signal pulses being received when said read and load clock signal pulses are eliminated.

7. The integrated circuit of claim 3 wherein each of said plurality of first junctions and said end junction includes a Josephson junction and an isolation inductor connected in a symmetrically arranged loop.

8. The integrated circuit of claim 1 wherein said data storage circuit further includes a plurality of logical zero junctions coupled to said clock-storage circuit for receiving a logical zero.

9. The integrated circuit of claim 8 wherein said logical zero junctions acknowledge an absence of said SFQ signal pulse in association with said load signal pulse.

10. The integrated circuit of claim 8 wherein said data storage circuit further includes a plurality of logical one junctions connected to said logical zero junctions for transmitting a logical one SFQ signal pulse.

11. The integrated circuit of claim 10 wherein said logical one junctions acknowledge said logical one SFQ signal pulse in association with said load clock signal pulse.

12. A superconductive integrated circuit comprising:

a clock storage circuit for receiving a plurality of load clock signal pulses from a first input port, wherein said clock storage circuit includes a plurality of stages for storing said load clock signal pulses; and

a data storage circuit coupled to said clock storage circuit for receiving and storing a plurality of data signal pulses in a sequential order of said data signal pulses being received in association with said load clock signal pulses, wherein said data signal pulses ripple through said plurality of stages along with said load clock signal pulses,

wherein previously stored load clock signal pulses provide back pressure to said load clock signal pulses that are subsequently stored and enable said clock storage circuit to store only one load clock signal pulse in each of said stages.

13. The integrated circuit of claim 12 wherein said clock storage circuit also receives a read clock signal pulse from a second input port.

14. The integrated circuit of claim 13 wherein each of said load and read clock signal pulses propagate through said plurality of stages that are empty towards said second input port and occupy a last stage that is empty.

15. The integrated circuit of claim 13 wherein said data storage circuit outputs said data signal pulse in accordance with said read clock signal pulse.

16. The integrated circuit of claim 13 wherein said load and read clock signal pulses are SFQ signals transmitted in the 10-100GHz range.

17. The integrated circuit of claim 12 wherein said clock storage circuit further includes:

a current source;

a plurality of first junctions coupled to said current source for receiving and storing said load clock signal, wherein one of said plurality of first junctions defines the first input port; and

an end junction connected to one of said plurality of first junctions for receiving and storing said load clock signal.

18. The integrated circuit of claim 12 wherein said data storage circuit further includes:

a plurality of logical zero junctions coupled to said clock storage circuit for receiving a logical zero data signal defining an absence of said data signal pulse in association with said load clock signal pulse; and

a plurality of logical one junctions coupled to said logical zero junctions for receiving a logical one data signal pulse in association with said load clock signal pulse.

19. An SFQ superconductive integrated circuit comprising:

a clock storage circuit for receiving load and read clock signal pulses from first and second input ports, wherein said clock storage circuit has a plurality of stages for storing said load clock signal pulses in an order of said load clock signal pulses being received; and

a data storage circuit coupled to said clock storage circuit for receiving and storing a plurality of data signal pulses in a sequential order of said data signal pulses being received in association with said load clock signal pulses, wherein said data signal pulses propagates through said plurality of stages in association with said load clock signal pulses, said data storage circuit outputs a first-received data signal pulse that is received prior to the other data signal pulses when said read clock signal pulse is received,

wherein previously stored load clock signal pulses provide back pressure to said load clock pulses being stored subsequently and enable said clock storage circuit to store only one signal pulse in each stage.

20. The integrated circuit of claim 19 wherein each of said load and read clock signal pulses are eliminated in one of said plurality of stages containing said first-received data signal pulse when said read clock signal pulse is received.